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High mobility ambipolar MoS₂ field-effect transistors: Substrate and dielectric effects

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We fabricate MoS₂ field effect transistors on both SiO₂ and polymethyl methacrylate (PMMA) dielectrics and measure charge carrier mobility in a four-probe configuration. For multilayer MoS₂ on SiO₂, the mobility is 30–60 cm²/Vs, relatively independent of thickness (15–90 nm), and most devices exhibit unipolar n-type behavior. In contrast, multilayer MoS₂ on PMMA shows mobility increasing with thickness, up to 470 cm²/Vs (electrons) and 480 cm²/Vs (holes) at thickness ~50 nm. The dependence of the mobility on thickness points to a long-range dielectric effect of the bulk MoS₂ in increasing mobility. © 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4789365>]

High quality two-dimensional materials have attracted significant attention due to their interesting physics and potential applications for electronic devices.¹ An outstanding example is graphene which has taken both the scientific and technological communities by storm.^{1–3} However, the absence of a bandgap^{4,5} inhibits its broader applications such as CMOS-like logic devices. Unlike graphene, MoS₂ has a thickness-dependent bandgap of 1.3–1.9 eV (Refs. 6–10) and is therefore promising for field-effect transistors (FETs). Indeed, recent studies of exfoliated thin MoS₂ on SiO₂ have demonstrated field-effect operation with high on-off ratios at room temperature.^{11–16} The 1.9 eV direct band gap of monolayer MoS₂ makes optoelectronic devices possible.^{8,17,18} On the other hand, bilayer and multilayer MoS₂ devices are also interesting: the bandgap of bi-layer MoS₂ is expected to be tunable by vertical electric field,^{19,20} and multilayer MoS₂ is expected to carry higher drive current than monolayer MoS₂ due to its lower band gap and triple of density of states at the conduction band minimum.^{15,16} A recent report of gate-tuned superconductivity at temperatures up to 9.4 K in multilayer MoS₂ adds further interest.²¹

The substrate and overlayer of a thin-film transistor may affect its performance through the introduction of disorder (either long-ranged charge disorder, or short-ranged disorder caused by chemical bonding or roughness) which reduce the charge carrier mobility, and by dielectric screening which may enhance the mobility.²² Previous studies of backgated exfoliated MoS₂ FET devices on bare SiO₂ found charge carrier mobility <50 cm²/Vs and large subthreshold swings (>1 V/decade).^{1,11,23} MoS₂ on Al₂O₃ substrates^{15,16} showed improved mobility (>100 cm²/Vs)¹⁵ and good subthreshold swings (70–80 mV/decade).¹⁵ Studies of MoS₂ on SiO₂ with various top gate schemes (HfO₂, Al₂O₃ and polymer electrolyte)^{12–14} reported much higher mobility values (>900 cm²/Vs) but it is likely that mobility was significantly overestimated in these dual-gated geometries.²⁴ However, it is also apparent that the addition of the superstrate dielectric enhanced the conductance of the MoS₂ devices. Hence, open questions remain as to the role of the dielectric substrate and overlayers in both causing and screening disorder in MoS₂ thin-film FETs.

In this paper, we report fabrication of MoS₂ FETs of varying thickness (1–80 nm) on both SiO₂ and polymethyl methacrylate (PMMA) dielectric substrates. For multilayer MoS₂ on SiO₂, the mobility is on order of 30–60 cm²/Vs consistent with previous results,¹¹ relatively independent of thickness, and most devices exhibit unipolar n-type behavior. In contrast, multilayer MoS₂ on PMMA shows mobility increasing with thickness, up to 470 cm²/Vs (electrons) and 480 cm²/Vs (holes) at thickness ~50 nm. The dependence of the mobility on thickness for thicknesses up to 80 nm is unexpected, and points to a long-range dielectric effect of the bulk MoS₂ in increasing mobility. Addition of a PMMA layer on top of the MoS₂ devices further increases the mobility, confirming the dielectric effect.

The starting substrates for device fabrication are 300 nm SiO₂ on Si, or spin-coated 300 nm PMMA on 300 nm SiO₂ on Si baked at 170 °C for 30 min. We choose PMMA as a polymer dielectric because of its easy deposition by spin coating, low values for the trapped charge density, and high dielectric constant similar to that of silicon dioxide (3.9 at 60 Hz). Thin films of MoS₂ were obtained by tape-cleavage of a single crystal geologic specimen of molybdenite (verified by both energy-dispersive X-ray spectroscopy and X-ray photoelectron spectroscopy to be single crystal 2H-type MoS₂) followed by mechanical exfoliation onto the device substrate.¹¹ Thin MoS₂ flakes are optically visible on such substrates, and among those we select the crystals that are as uniform as possible by examining optical microscope and atomic force microscope (AFM) images. Thickness *t* of the flakes is measured by AFM. Four-probe electrical contacts (30 nm Ti and 80 nm Al) are patterned on top of selected MoS₂ flakes using a shadow mask technique,²⁵ avoiding contamination by residues from chemical resists or developers. The conductivity σ is measured in a four-probe configuration as a function of carrier density $n = c_g V_g$ where c_g is the back-gate capacitance per unit area, and V_g is the back-gate voltage. The potential difference across the voltage probes is kept below 100 mV in all measurements. In the four-probe configuration with a single back-gate electrode, the charge-carrier mobility is well approximated by the field-effect mobility $\mu_{FE} = \frac{1}{e} \frac{d\sigma}{dn}$, where e is the elementary charge. By

examining both two-probe and four-probe conductivity measurements (electrical setup as shown in Fig. 1(a)), we observe that the contact resistance varies from sample to sample, and is especially large ($\sim M\Omega$) for thin flakes (<3 nm); the four-probe geometry eliminates contributions from contact resistance which could cause the conductance to be significantly underestimated.

Fig. 1(a) shows a schematic of our four-probe devices, and Fig. 1(b) shows an optical micrograph of a typical PMMA-supported MoS₂ device. Figures 1(c) and 1(d) display the room temperature four-probe conductivity σ as a function of applied back gate voltage V_g for four devices with thickness of 1.5, 6.5, 47, and 80-nm, respectively, which summarize the range of observed device behaviors and demonstrate the qualitative trends observed with increasing device thickness. The 1.5-nm-thick device (bilayer MoS₂) displays an *n*-type unipolar behavior indicated by turning on of conductivity at positive V_g (accumulation of electrons), while staying off at a window of negative V_g , which agrees with previously reported MoS₂ FETs on SiO₂. The 6.5 nm thick device shows clear ambipolar behavior in Fig. 1(d), but with much lower mobility (~ 1 cm²/Vs) for holes compared to electrons (68 cm²/Vs). Note that in the four-probe setup, the lower mobility is not an artifact due to contact resistance, but reflects the bulk carrier mobility. The 47-nm-thick device shows good ambipolar behavior with high mobility for electrons and holes (~ 270 and 480 cm²/Vs, respectively). A trend towards

a smaller window of off state (separating the electron and hole conduction regions) and higher off-state conductance is observed with increasing thickness, and by $t = 80$ nm there is no clear separation of electron conduction, off, and hole conduction regions indicating that carriers in the bulk of the MoS₂ are likely dominating the conductance.

Figure 2 plots room temperature μ_{FE} as a function of thickness t for all measured MoS₂ flakes. To shed light on the ambipolar behavior and thickness dependence of MoS₂ devices, we systematically investigated more than 50 PMMA-supported devices and 6 SiO₂-supported devices, with thickness spanning from monolayer to 150 nm. We exclude the thick MoS₂ devices that show bulk behavior (e.g., $t = 80$ nm in Figs. 1(c) and 1(d)) and include only devices with a clear off state. Devices with ambipolar performance are indicated as dashed-line connected hollow squares (corresponding hole-carrier mobility) and solid squares (corresponding electron-carrier mobility). To avoid dielectric breakdown, the range of V_g for PMMA-supported devices is ± 150 V and ± 75 V for SiO₂-supported devices. Most of the PMMA-supported thin devices (monolayer–30 nm) and all SiO₂-supported devices display *n*-type unipolar behavior, while ambipolar performance is observed in most PMMA-supported thick devices (40 nm $< t < 70$ nm) with high-mobility.

The mobility of PMMA-supported MoS₂ devices show an increasing trend with thickness, up to 470 cm²/Vs

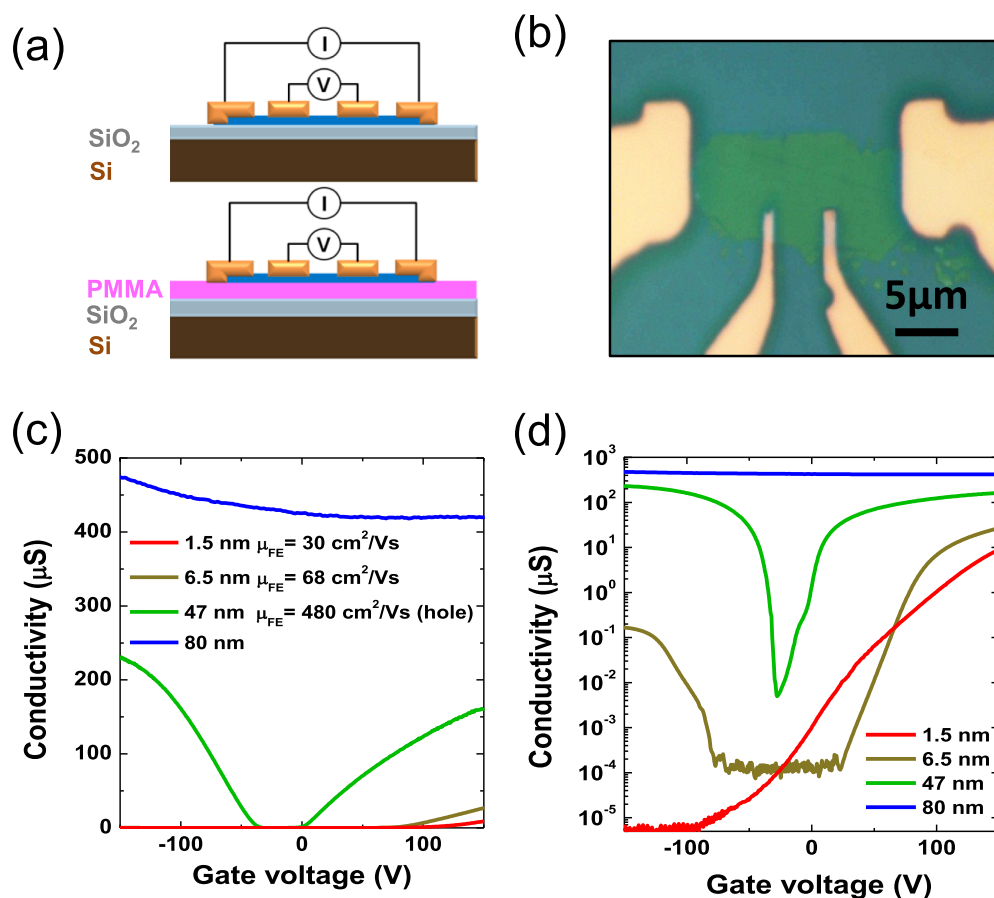


FIG. 1. (a) Schematics of four-probe MoS₂ devices on SiO₂/Si and PMMA/SiO₂/Si. (b) Optical image of a typical PMMA-supported MoS₂ device. Green area is MoS₂ flake, yellow areas are Ti/Al electrodes, and blue area is the PMMA/SiO₂/Si substrate. (c–d) Conductivity σ as a function of gate voltage V_g on linear (c) and semi-logarithmic (d) scales for four MoS₂ devices on PMMA with thickness of 1.5 (red), 6.5 (brown), 47 (green), and 80 nm (blue).

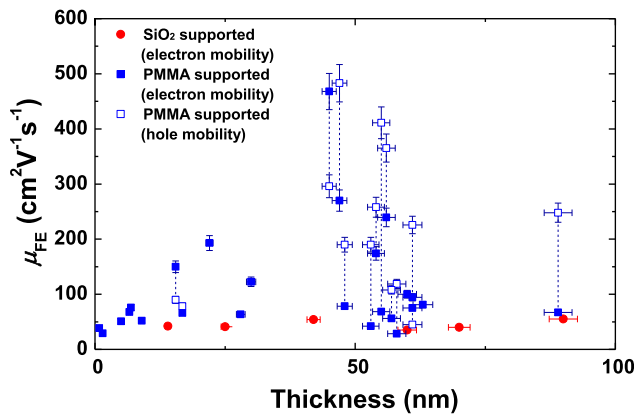


FIG. 2. Room temperature field effect mobility μ_{FE} as function of thickness t for 25 PMMA-supported (blue squares) and 6 SiO₂-supported MoS₂ (red circles) devices. Only electron mobility is shown for SiO₂-supported devices. PMMA-supported devices with measurable ambipolar behavior are indicated as dashed-line connected hollow squares (corresponding hole-carrier mobility) and solid squares (corresponding electron-carrier mobility).

(electrons) and 480 cm²/Vs (holes) for thicknesses near 50 nm. In most devices with ambipolar behavior, the mobility is larger for holes than for electrons, suggesting that p -type operation is more favorable for multilayer MoS₂ FETs. In contrast, the mobility of SiO₂-supported devices is much lower (30–60 cm²/Vs) and almost thickness independent, and ambipolar behavior is rarely observed in them. Our observed mobilities are the highest four-probe room-temperature mobilities measured in MoS₂, comparable to the room temperature intrinsic hole mobility in silicon, and somewhat higher than existing estimates of phonon-limited room temperature mobility for thick¹⁵ and single-layer MoS₂.²⁶ Notably, the highest electron and hole mobilities are comparable, an advantageous property for CMOS, possibly reflecting the similar electron and hole masses in MoS₂.⁹ The observed room temperature mobilities are also the highest of which we are aware in any ambipolar thin-film field-effect device with the exception of graphene.

The observation of a thickness-dependent mobility in MoS₂ up to thickness of 50 nm or more is surprising. Confinement effects on the bandgap are negligible beyond a few nm thickness,^{8–10} and the carriers in MoS₂ FETs are expected to be confined within a few nm of the gate dielectric interface.¹⁵ The thickness dependence points to a role for the additional MoS₂ above this region which contains few charge carriers. One possible explanation is that the additional MoS₂ layers serve as a dielectric capping layer which enhances screening of long-range disorder. To test this hypothesis, we add an additional dielectric layer (spin-coated PMMA, thickness of 300 nm) to most of the measured devices shown in Fig. 2 and re-measured the mobility. The results are plotted in Fig. 3(a) (only the higher of hole or electron mobility is plotted for devices with ambipolar behavior). Top-coating with PMMA enhances the mobility of most PMMA-supported devices, even those of thickness ~60 nm (maximum improvement of more than 300%), while SiO₂-supported devices only show a slight increase of mobility. Typical device output characteristics before and after double layer PMMA coverage are shown in Figs. 3(b) and 3(c) for PMMA-supported and SiO₂ supported MoS₂,

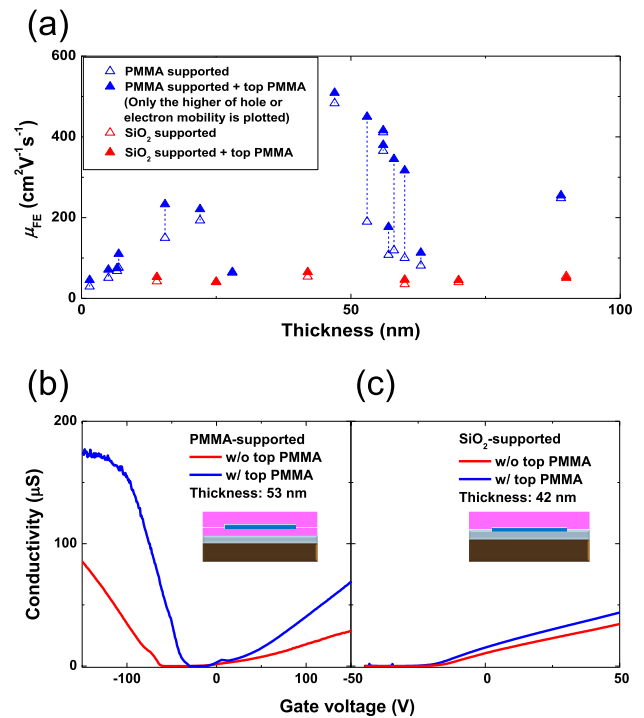


FIG. 3. (a) Thickness-dependent field effect mobility $\mu_{FE}(t)$ of PMMA (blue) and SiO₂ (red) support MoS₂ before (hollow triangles) and after (solid triangles) additional PMMA top-coating for most devices measured in Fig. 2. Only the higher of hole or electron mobility is plotted for devices with ambipolar behavior. (b–c) Typical $\sigma(V_g)$ characteristics before (red curve) and after (blue curve) PMMA top-coating for a PMMA-supported device (b) and a SiO₂-supported device (c) Insets: schematic views of devices after top-coating of PMMA.

respectively. The results confirm that additional dielectric layers can enhance the mobility of MoS₂ on PMMA even for MoS₂ thicknesses of 60 nm, demonstrating the importance of long-range disorder in determining the mobility of MoS₂ on PMMA. For lower-mobility MoS₂ on SiO₂, the effect of increasing MoS₂ thickness or adding additional PMMA dielectric is small, indicating the dominance of short range disorder, likely chemical bonding to SiO₂ or interface roughness scattering.

In conclusion, we study the dependence of MoS₂ field effect mobility on substrate (SiO₂ and PMMA), MoS₂ thickness, and PMMA dielectric overlayer. MoS₂ on SiO₂ shows typically unipolar n -type behavior, low mobility relatively independent of MoS₂ thickness or dielectric overlayer. PMMA-supported devices show ambipolar behavior with the highest measured room temperature four-probe mobilities for MoS₂, increasing with thickness (comparable to p -type silicon; up to 470 cm²/Vs for electrons and 480 cm²/Vs for holes at thickness ~50 nm). For MoS₂ on PMMA mobility could often be improved even further by covering device surface with an extra top layer of PMMA. The strong dielectric effects on mobility for MoS₂ devices on PMMA imply a dominance of long-range disorder, while the absence of such effects for MoS₂ on SiO₂ implies a dominance of short-range disorder at the SiO₂ interface due to chemical bonding or surface roughness.

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