nature electronics

Article

https://doi.org/10.1038/s41928-023-00971-7

Wafer-scale transistor arrays fabricated using slot-die printing of molybdenum disulfide and sodium-embedded alumina

Received: 3 November 2021

Accepted: 27 April 2023

Published online: 08 June 2023

Check for updates

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Two-dimensional materials made via solution processing could be used to create next-generation electronic devices at scale. However, existing solution processing methods typically have a trade-off between scalability and material quality, which makes them unsuitable for practical applications. Here we show that wafer-scale arrays of molybdenum-disulfide-based transistors can be fabricated using a commercial slot-die printing process. We create inks of molybdenum disulfide nanosheets and sodium-embedded alumina for printing of the semiconductor and gate dielectric layer, respectively. The transistors exhibit average charge carrier mobilities of 80.0 $cm^2 V^{-1} s^{-1}$ in field-effect transistor measurements and 132.9 $cm^2 V^{-1} s^{-1}$ in Hall measurements at room temperature. The high charge carrier mobility is attributed to the sodium-embedded alumina gate dielectric, which causes a band-like charge carrier transport in the molybdenum-disulfide-nanosheet-based thin-film networks. We use the transistors to create various logic gates, including NOT, NOR, NAND and static random-access memory.

Solution-based processing of low-dimensional materials is a potential route to the scalable production of electronic devices in a cost-effective manner[1–8]. Typically, wet chemistry is used to form an ink where the desired low-dimensional material is stabilized in a solvent[4,5,7–11] and then deposited on a target substrate using different coating methods (such as spin coating, spray coating, vacuum filtration and inkjet printing)[4,5,11–13]. Two-dimensional (2D) nanosheets are particularly attractive as a solution-processable material for use in large-scale electronics due to their atomically clean and dangling-bonds-free surfaces. This makes the formation of van der Waals contacts with neighbouring nanosheets feasible and can result in thin-film networks with minimal charge transport loss at the interfaces[6,11,14].

The 2D semiconductor molybdenum disulfide (MoS_2) has been intensively studied as a material for electronic devices due to

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https://doi.org/10.1038/s41928-023-00971-7

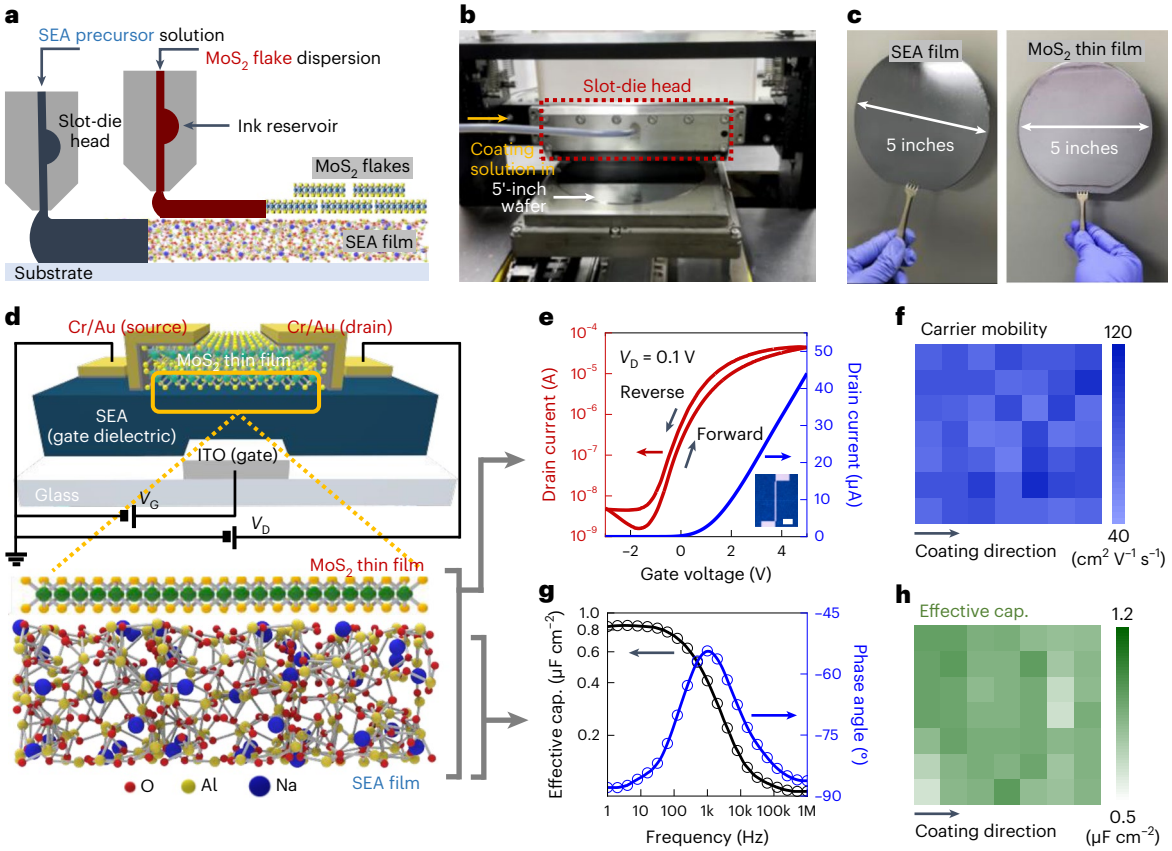

Fig. 1 | Device fabrication based on slot-die coating. a, Schematic of the slot-die coating of SEA and MoS_2. **b**, Optical image showing the slot-die coating setup for consecutive wafer-scale coating. **c**, Image of slot-die-coated SEA and MoS_2 on a 5-inch silicon wafer. **d**, Schematic of SEA-gated MoS_2 TFT and the atomic structure of MoS_2 thin film and SEA layer. **e**, Transfer characteristics and optical microscopy image (inset) of the SEA-gated MoS_2 TFT. The channel length and width are 10 and 10 μm, respectively. Scale bar, 300 μm. **f**, Colour map of carrier mobility distribution. **g**, Capacitance (left) and phase angle (right) properties of SEA with different frequencies. **h**, Colour map of the effective capacitance distribution.

its combination of physical, chemical and optical properties[6,11,15,16]. However, there is a trade-off between the scalable synthesis of MoS_2 and material quality, which limits its use in practical applications. For example, liquid-phase exfoliation can produce large amounts of dispersed MoS_2 nanosheets, but these sheets have a small lateral size (less than 100 nm) and a broad thickness distribution that hinders the formation of electrically conductive thin-film structures[4,9,16]. Molecular-intercalation-based electrochemical exfoliation can produce nanosheets of MoS_2 with highly uniform thicknesses and relatively large sizes (more than 1 μm)[6,11,14]. However, although electrochemically exfoliated MoS_2 nanosheets can create electrically active thin films with gate tunability, their field-effect mobility is limited to below 10 $cm^2 V^{-1} s^{-1}$ at room temperature[6,11]. This value is comparable with that of micromechanically exfoliated MoS_2-based transistors fabricated on conventional SiO_2/Si substrates, but is far lower than the phonon-scattering-limited field-effect mobility of bulk MoS_2 (200–500 $cm^2 V^{-1} s^{-1}$ at room temperature[17]).

One way to improve the field-effect mobility of solution-processed MoS_2 thin films is by using high-κ dielectric layers, such as hafnium oxide (HfO_2) and aluminium oxide (Al_2O_3) (refs. 11,12,15,18,19). For example, it has been shown that introducing an atomic layer deposition (ALD)-grown layer of HfO_2 as a high-κ gate dielectric can increase the average field-effect mobility of micromechanically exfoliated MoS_2 nanosheets by two orders of magnitude[20]. However, although ALD can produce dielectric layers over large areas with high quality, the process is limited by slow deposition rates and difficulties controlling the doping due to complex reactions between the precursors[21].

In this article, we report a wafer-scale solution-processed MoS_2 thin-film transistor (TFT) array with an average field-effect electron mobility at room temperature of 80.0 $cm^2 V^{-1} s^{-1}$. Consecutive slot-die printing of layers of sodium-embedded alumina (SEA) and MoS_2 nanosheet inks is used to create uniform and wafer-scale gate dielectric and semiconductor layers, respectively. Temperature-dependent charge transport and scanning probe microscopy measurements show that the high electron mobility of the MoS_2-on-SEA structure can be attributed to the band-like charge transport occurring through well-percolated MoS_2 thin films, which have effective van der Waals sheet-to-sheet contacts, as well as an energetically flat SEA dielectric layer. We use our slot-die-printed MoS_2-on-SEA transistors to create various logic gates—NOT, NOR, NAND and static random-access memory (SRAM)—at the wafer scale.

Device fabrication based on slot-die coating

To achieve the wafer-scale fabrication of MoS_2-based TFT arrays, SEA precursor solutions and MoS_2 nanosheet dispersions are sequentially coated on an arbitrary rigid substrate using a slot-die coating method (Fig. 1a) (Supplementary Figs. 1 and 2 show the photographs of the as-prepared dispersions, MoS_2 sheet morphology and films coated on transparent glass substrates). A photograph of the slot-die coater for preparing wafer-scale electronics is shown in Fig. 1b, which is an effective scalable process to yield large-area thin films with good uniformity and reliability. Therefore, this approach can be readily implemented in industry compared with other solution-based coating methods. First, the SEA precursor solution was carefully injected into the head

of the coater at a constant rate of 2.5 ml min^{-1} and ejected through the nozzle placed at the bottom of the head. As the solution is ejecting, the slot-die head simultaneously moves in the x–y directions at a constant rate of ~10 mm s^{-1} for a homogeneous coating of SEA on the substrate. Subsequently, MoS_2 dispersion was coated in a similar manner to form a semiconducting layer on the SEA layer (Supplementary Video 1). For the successful formation of the semiconducting layer, MoS_2 dispersion was prepared by molecular-intercalation-driven electrochemical exfoliation followed by a mild bath sonication in a solvent. The resulting MoS_2 samples possess a semiconducting 2H phase (Supplementary Fig. 3). Photographs taken after each layer coating on a 5-inch silicon wafer are shown in Fig. 1c. The resulting MoS_2/SEA layers were used to fabricate a conventional TFT structure (Fig. 1d), where the corresponding atomic structures of the MoS_2 sheet and SEA are represented. A representative electrical transfer curve of the TFT on a semi-logarithmic scale (red curves) and a linear scale (blue curve) is shown in Fig. 1e. As the gate voltage (V_G) changes to positive values, the drain current abruptly turns on at $V_G \approx 0$ V with an on/off ratio exceeding 5×10^4 and a negligible hysteresis loop between the forward and reverse sweeps. The corresponding output curve exhibits a typical n-type TFT behaviour, showing both linear and saturation drain voltage (V_D) dependence (Supplementary Fig. 4). From the transfer characteristics, field-effect carrier mobility values are extracted based on the equation $I_D = V_D C_i \mu W(V_G - V_{th})/L$, where I_D is the drain current; C_i is the effective capacitance of the gate insulator; V_{th} is the threshold voltage; and L and W are the channel length and width, respectively. Note that the value for C_i was carefully measured from the metal–insulator–semiconductor testbeds consisting of vertically stacked indium tin oxide (ITO)–SEA–MoS_2 films, as schematically illustrated in Supplementary Fig. 5. From the structure, the specific capacitance value is obtained as 1.19 ± 0.11 μF cm^{-2}, which is used to calculate the carrier mobilities from the field-effect transistor measurements. The carrier mobilities of 49 TFTs in a fabricated array are displayed in a 2D mapping image (Fig. 1f), which shows high spatial homogeneity with an average value of 80.0 ± 11.0 $cm^2 V^{-1} s^{-1}$ at room temperature (the transfer curves of all the 49 devices are shown in Supplementary Fig. 6). A comparison with other reported field-effect mobilities of wafer-scale MoS_2-based TFTs is shown in Supplementary Fig. 7 and Supplementary Table 1. The colour maps and statistics of carrier mobility, turn-on voltage and current on/off ratio are shown in Supplementary Figs. 8 and 9. Furthermore, the operational and environmental stabilities of the devices are shown in Supplementary Figs. 10 and 11.

To fully elucidate the dielectric properties of the slot-die-coated SEA dielectric layer, the capacitive properties of SEA were investigated using a simple metal–insulator–metal testbed structure (that is, Si^{++}/SEA/Cr/Au electrode). The resulting frequency-dependent capacitance and phase angle, measured by impedance spectroscopy, are shown in Fig. 1g. In particular, the specific capacitance measured at 1 Hz is 0.84 μF cm^{-2}, which is 17 times higher than that of an Al_2O_3 dielectric with a comparable thickness[19] (~0.05 μF cm^{-2}). To explore the origin of such high capacitance, frequency-dependent capacitance measurements were performed. The capacitance is nearly constant when the frequency increases up to 100 Hz and then gradually decreases as the frequency increases further. Over the same frequency range, the measured phase angle is initially at −90°, then increases towards 0° and eventually returns to −90° at higher frequencies, which implies that the dominant working mechanism changes from capacitive (−90°) to resistive (towards 0°) and back to capacitive modes, respectively[22–25]. These frequency-dependent capacitance and phase angle changes indicate that the embedded Na^+ ions effectively contribute to charging at low frequencies (capacitive mode), but due to limited response time for the displacement of Na^+ ions (resistive mode), the capacitance decreases[26–28]. In the high-frequency regime beyond the timescale of Na^+-ion motion, the measured capacitance values eventually become ~0.1 μF cm^{-2}, which is close to the reported capacitance of pristine Al_2O_3 operating purely based on dipolar relaxation. Figure 1h shows the distribution of 49 capacitance measurements, where the colour intensity indicates the value of the measured capacitance and the x and y axes designate the spatial positions. Based on the spatial mapping, an average capacitance value of 0.84 ± 0.07 μF cm^{-2} was shown with high spatial uniformity. In addition, a series of dielectric and structural properties including breakdown voltage, leakage current, thickness and surface roughness are shown in the spatial mapping images (Supplementary Figs. 12–14).

Device optimization and origin of high carrier mobility

Based on the SEA layer possessing a high average capacitance, we further optimized the device performance by controlling the fabrication conditions. As illustrated in Fig. 1, SEA and MoS_2 layers are sequentially coated via slot-die coating, and subsequently, the MoS_2 layer is chemically doped by exposure to bis(trifluoromethane) sulfonimide (TFSI) followed by heat treatment (Fig. 2a). The resulting electrical transfer characteristics are shown in Fig. 2b after each step (that is, MoS_2 coating, TFSI treatment and heat treatment). First, the MoS_2 ink concentrations were varied from 1 to 3 mg ml^{-1} to optimize the slot-die-coated channel thickness (Supplementary Fig. 15). The optimized channel thickness was ~15 nm, which was prepared from the 2 mg ml^{-1} ink, leading to the best device performance (Supplementary Fig. 16). Although the as-coated MoS_2 thin film shows a current on/off ratio of ~7×10^2, subthreshold swing of 1.58 V dec^{-1} and V_{th} of 0.16 V with a heavily n-doped electrical behaviour due to the sulfur vacancies formed during processing (grey line), unintentional doping is greatly suppressed by TFSI-assisted chemical treatment (black line) (Supplementary Fig. 16). After the chemical treatment, the transfer characteristics substantially changed, with the current on/off ratio of ~10^5, subthreshold swing of 0.32 V dec^{-1} and positively shifted V_{th} of 3.23 V. More importantly, the chemical treatment boosted the electron mobility from 4.7 to 18.9 $cm^2 V^{-1} s^{-1}$. As previously reported, TFSI molecules play a role to passivate sulfur vacancies on the basal plane of MoS_2 nanosheets, which act as carrier-trapping sites[6,29]. Also, the charge density of MoS_2 is reduced because the TFSI molecules serve as a Lewis acid to withdraw electrons[30]. Consequently, for the TFSI-treated MoS_2 device, the subthreshold swing is improved by around five times and V_{th} is shifted towards a positive direction (from 0.16 to 3.23 V) compared with those of the as-coated MoS_2 thin-film counterpart. The electrical characteristics corresponding to the TFSI treatments with various concentrations are shown in Supplementary Fig. 17. A comprehensive suite of characterizations including Kelvin probe force microscopy (KPFM), Raman spectroscopy, photoluminescence spectroscopy and X-ray photoelectron spectroscopy is also performed to study the effect of TFSI concentration on the properties of the MoS_2 thin film (Supplementary Figs. 18–20). Following the chemical treatment, an additional annealing process further improved the MoS_2 nanosheet-to-nanosheet contact and removed the residual solvent. Consequently, the resulting current level increased by at least one order of magnitude at the applied gate voltage of 5 V (Fig. 2b, red line). The transfer characteristics at various annealing temperatures (100, 150, 200, 250 and 300 °C) are plotted in Supplementary Fig. 21a. As the annealing temperature increases up to 250 °C, the on current increases and V_{th} becomes negative, but the device performance is slightly degraded after annealing at 300 °C. The decreased carrier mobility and increased off current of the device annealed at 300 °C are possibly due to the partial oxidation of MoS_2 to MoO_x (refs. 6,11). The corresponding carrier mobility and current on/off ratio as a function of annealing temperature are plotted (Supplementary Fig. 21b), and the corresponding characterizations are shown in Supplementary Figs. 22 and 23. We note that the device characteristics and carrier mobility values (Fig. 1) are obtained from the MoS_2 channels that underwent the TFSI-based chemical treatment and subsequent annealing. Such high field-effect mobility values were

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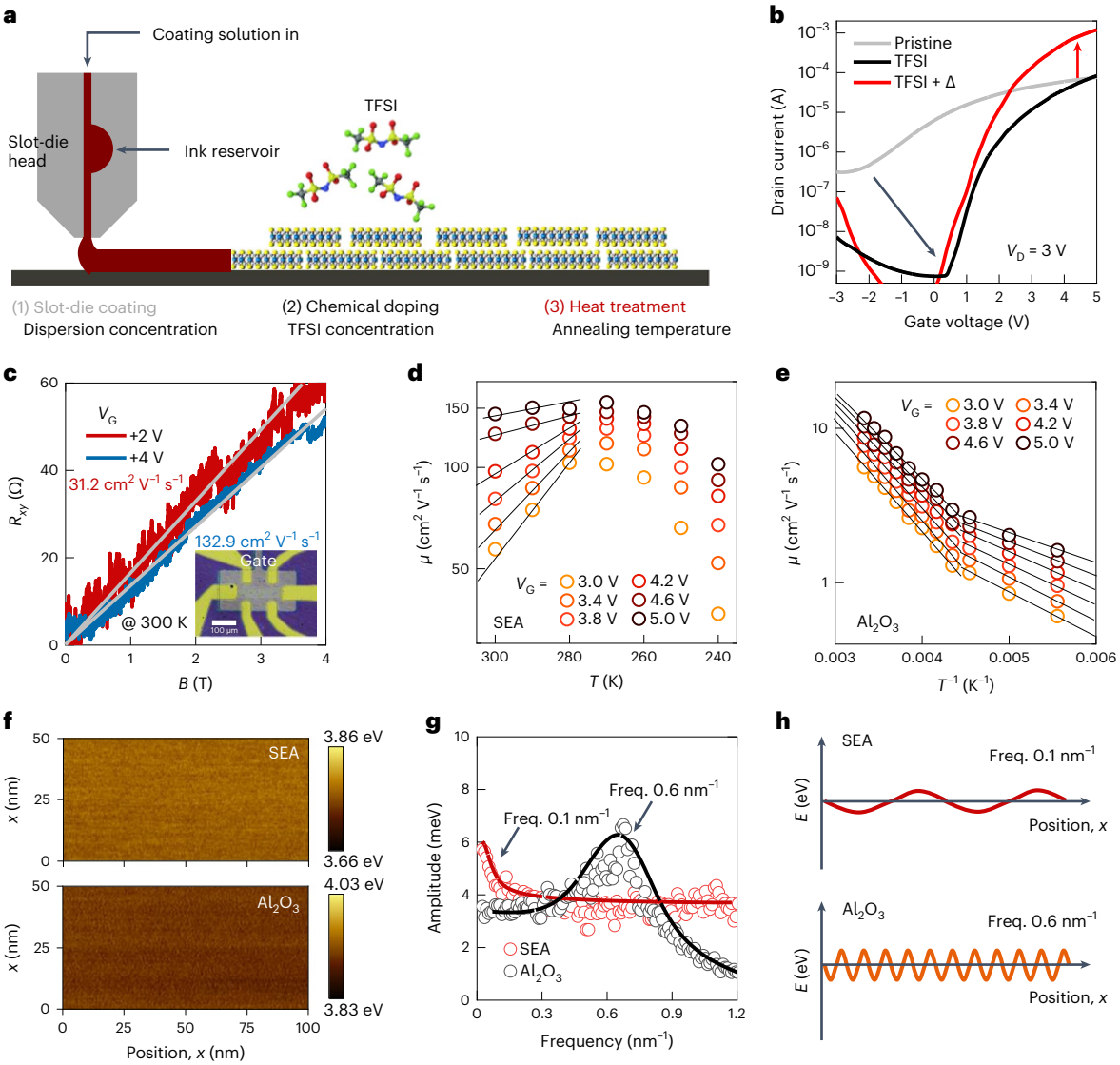

Fig. 2 | Device optimization and origin of high carrier mobility. a, Schematic of the optimized treatment process for the MoS_2 semiconductor film. **b**, Electrical transfer characteristics of TFTs with a pristine MoS_2 film, after TFSI treatment and after TFSI treatment and thermal annealing. **c**, Hall measurements of SEA-gated device; the inset shows the optical image of the Hall bar device (scale bar, 100 μm). **d**, Carrier mobility plotted with respect to temperature for SEA-gated MoS_2 TFTs measured at different gate voltages. **e**, Carrier mobility plotted against inverse temperature for ALD-deposited Al_2O_3-gated MoS_2 TFTs measured at different gate voltages. The 2D variable-range hopping fitted lines (low-temperature region) and nearest-neighbour hopping fitted lines (high-temperature region) are shown for each gate voltage. **f**, KPFM images representing the spatial distribution of work functions of SEA and solution-processed Al_2O_3. **g**, Line profile of the fast Fourier transform results of the KPFM image. **h**, Schematic of the energetic line profiles of SEA and solution-processed Al_2O_3 surfaces.

further evaluated by Hall measurements under the application of gate voltages (Fig. 2c). Each Hall mobility value of 31.2 and 132.9 $cm^2 V^{-1} s^{-1}$ at $V_G = 2$ V (red) and 4 V (blue), respectively, is comparable with the field-effect mobility value at the corresponding V_G. A schematic of the Hall bar device is shown in Supplementary Fig. 24.

To further elucidate the origin of the ultrahigh carrier mobility of our optimized solution-processed MoS_2-based TFTs, the carrier transport measurements were performed at various temperatures (T) (Supplementary Figs. 25 and 26). As control experiments, temperature-dependent transfer characteristics of the same MoS_2 samples were evaluated on a conventional alumina (Al_2O_3) dielectric without sodium, which were prepared either by ALD or solution processing (spin coated) (Supplementary Fig. 27). These MoS_2 TFTs based on alumina dielectrics show an average carrier mobility of ~10 $cm^2 V^{-1} s^{-1}$, which is comparable with the previously reported value[6,11]. Figure 2d,e shows the T-dependent mobility variation obtained from an SEA-gated MoS_2 TFT and a solution-processed Al_2O_3-gated MoS_2 TFT, respectively (Supplementary Fig. 28 shows the data for ALD-deposited Al_2O_3-gated MoS_2 TFT). Not only is a large difference in the absolute mobility values reconfirmed between the two devices over the entire temperature range but also the T dependencies of the two devices were evident. In particular, the SEA-gated MoS_2 layer yielded completely different T dependence in two different temperature regimes. Below 270 K, mobility increases as the temperature increases, whereas mobility decreases as the temperature increases above 270 K. The positive mobility versus temperature correlation indicates thermally assisted hopping-type transport through the film. Hopping transport has been widely observed from various solution-processed MoS_2 nanosheet systems, which is limited by the energy needed for inter-nanosheet transport in the channel[13,31]. From the slope of the Arrhenius-type plot

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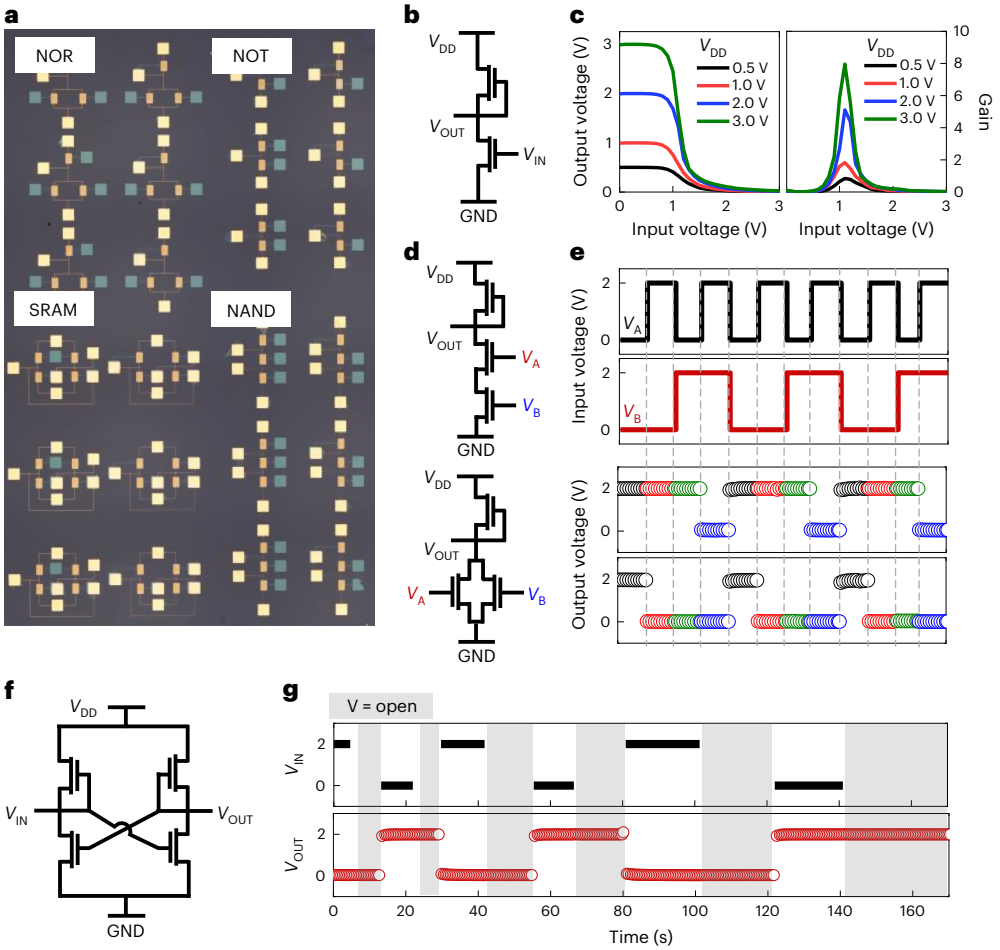

Fig. 3 | Applicability to large-area logic circuits. a, Optical image of NOR, NOT, NAND and SRAM logic gates. **b**, Circuit diagram of the NOT gate (inverter). **c**, Voltage transfer characteristics (left) and resulting voltage gain (right) of the NOT gate. **d**, Circuit diagrams of the NAND (top) and NOR (bottom) gates. **e**, Input voltage signals (top) and the corresponding output voltage signals (bottom) of the NAND and NOR gates. **f**,**g**, Circuit diagram (**f**) and input voltage signals and the corresponding output voltage signals of the SRAM gate (**g**). The shaded regions in **g** indicate completely open input signals.

shown in Fig. 2d, the activation energy for the SEA-gated MoS_2 layer at $T < 270$ K ranged from 234 to 91 meV depending on V_G. Note that the temperature-dependent transport study could not be conducted at $T < 240$ K, because the Na^+-ion motion was completely frozen at such low temperatures.

The negative mobility versus temperature correlation, on the other hand, is a typical signature of band-like transport that is based on the formation of highly extended electronic states where the conduction is limited by scattering processes[32–34]. We attribute the achievement of band-like transport and the associated high mobility values from our SEA-gated MoS_2 nanosheet films to the following key contributions. The first is the dimension of the solution-processed MoS_2 nanosheets we used; the lateral size and thickness of MoS_2 were 0.88 ± 0.42 μm and 2.8 ± 1.0 nm, respectively, which enables an effective plane-to-plane contact formation with negligible contact resistance via van der Waals interactions between individual MoS_2 nanosheets[6,11,14]. This aspect alone, however, cannot completely describe the formation of an extended energy band from the SEA-gated MoS_2 nanosheet films, because the same MoS_2 nanosheet films gated with Al_2O_3 yielded a mobility of ~10 $cm^2 V^{-1} s^{-1}$ without the negative mobility versus temperature correlation (Fig. 2e); the transport behaviours of the Al_2O_3-gated MoS_2 nanosheet films follow a thermally activated hopping process over the temperature range we examined (a transition between the nearest-neighbour hopping transport to 2D variable-range hopping was observed, consistent with previous reports[13,35,36]). The second important contribution is the energetic smoothness of the SEA surface. From a KPFM analysis, we found that the SEA surface has an energetically flat landscape. Figure 2f shows a spatial mapping of the work function distribution for the SEA (top image) and Al_2O_3 (bottom image) surfaces measured. The KPFM mapping images were then analysed using a fast Fourier transformation (Fig. 2g). In the case of SEA, the characteristic frequency (yielding the peak amplitude) is ~0.1 nm^{-1}, whereas that of Al_2O_3 is ~0.6 nm^{-1}. Considering that the maximum amplitudes of oscillation for both SEA and Al_2O_3 are similar (around ~6 meV), the smaller characteristic frequency value for the SEA surface indicates that its energetic landscape fluctuates more slowly over a longer length scale than that of Al_2O_3 (Fig. 2h). Therefore, we speculate that our SEA dielectric layer effectively provides an energetically smoother interface with an MoS_2 layer, and consequently, this allows the formation of extended energy states that enables band-like charge transport[37]. In addition to these contributions, the high-κ characteristics of SEA would also boost the carrier mobility by efficiently suppressing charge screening in very thin 2D materials[20,38]. Overall, we conclude that the combination of these factors enables the generation of high mobility values through band-like transport from the SEA-gated MoS_2 nanosheet films.

Applicability to large-area logic circuits

To verify the applicability of the SEA-gated MoS_2 TFTs to large-area electronics, various logic circuits were demonstrated including NOT,

NOR, NAND and SRAM (Fig. 3a). The circuit diagram of the NOT gate (inverter) is shown in Fig. 3b, where two identical MoS_2 TFTs are used as both driver and load transistors. Voltage transfer characteristics at different supply voltages (V_{DD}) and the resulting signal gains are shown in Fig. 3c. When an output voltage has the same value as the supply voltage at low input voltages (close to 0 V), the corresponding logic state is denoted as '1'. The output voltage decreases to 0 V as the input voltage increases, which corresponds to the logic state '0'. This inversion of the output voltage indicates the stable operation of the NOT gate, where the signal gain (absolute value of dV_{OUT}/dV_{IN}) value is higher than 7. Figure 3d shows the circuit diagrams of NAND and NOR gates. Both NAND and NOR gates are demonstrated by the implementation of three identical MoS_2 TFTs; all three are in series for the NAND gate and two in parallel and one in series for the NOR gate. In the NAND gate, the output voltage is 2 V (logic state '1'), if at least one of the input voltages is 0 V (logic state '0'). The output voltage is 0 V (logic state '0'), only if both input voltages are 2 V (logic state '1'). For the NOR gate, the output is at logic state '1' only if both inputs are at logic state '0'. Otherwise (that is (1,0), (0,1), (1,1)), the output logic state is at '0'. The output voltages with respect to the two input voltages for both NAND (top) and NOR (bottom) gates are shown in Fig. 3e. Both NAND and NOR gates steadily and repeatedly generate the expected output logic states for all the possible input combinations. Finally, SRAM logic gates composed of two cross-connected inverters are demonstrated (Fig. 3f). In an SRAM cell, each output of one inverter is connected to the input of the other inverter. If the initial input voltage (low or high) is applied to an inverter, the resulting output voltage (logic state '1' or '0') is fed to the input of the cross-connected inverter. Then, the output logic state of the cross-connected inverter is equal to the initially applied input, which is looped back into the initially operated inverter. Thus, an SRAM cell can maintain its output level even after the input is completely opened. Figure 3g exhibits the operation of the SRAM at various input voltages and time spans, where the shaded regions indicate completely open input states. The complete maintenance of the output states at the open input states (shaded regions) indicates the stable operation of our SRAM cell.

Conclusions

We have reported the large-scale, solution processing of MoS_2 electronics on a five-inch wafer using consecutive slot-die printing of MoS_2 nanosheet and SEA inks for the semiconductor and gate dielectric layers, respectively. The MoS_2-on-SEA TFTs exhibit field-effect and Hall mobility values of 80.0 and 132.9 $cm^2 V^{-1} s^{-1}$ at room temperature, respectively, as well as high spatial uniformity. We primarily attribute the origin of the high carrier mobility to the band-like transport behaviour of the MoS_2 thin films. The solution-processed transistors were used to create various logic circuits including NOT, NAND, NOR and SRAM. Our approach provides a potential route to high-performance, large-area electronics based on solution-processed 2D materials.

Methods

Device fabrication

To prepare SEA precursor solutions, aluminium nitrate nonahydrate (98.0%, Sigma-Aldrich) and sodium hydrogen sulfate (Sigma-Aldrich) mixed in a molar ratio of 10:2 were dissolved in a binary solvent of ethanol (anhydrous, Sigma-Aldrich) and acetone (99.5%, Sigma-Aldrich) (volume ratio, 6:1). The final concentration was 0.6 M. Precursor solutions for Al_2O_3 dielectrics were prepared by dissolving aluminium nitrate nonahydrate (98.0%, Sigma-Aldrich) in 2-methoxyethanol (anhydrous, 99.8%, Sigma-Aldrich) at a concentration of 0.5 M. Both solutions were stirred with a magnetic bar for 24 h at 65 °C. MoS_2 dispersion was prepared by electrochemical exfoliation with molecular intercalants. First, we constructed a two-electrode electrochemical cell using 50 mg of MoS_2 crystal (HQ Graphene) and graphite rod as the cathode and anode, respectively. Tetraheptylammonium bromide (99.0%, Sigma-Aldrich) dissolved in acetonitrile (anhydrous, 99.8%, Sigma-Aldrich) served as an electrolyte (concentration, 5 mg ml^{-1}). To intercalate the THA^+ ions into the MoS_2 crystal, a negative voltage of 7 V was applied to the cell for 1 h. After the electrochemical reaction, the as-intercalated crystal was rinsed with ethanol before sonication in polyvinylpyrrolidone (40,000 g mol^{-1}, Sigma-Aldrich) solution in dimethylformamide (5 ml; 22.2 mg ml^{-1}) for 30 min. To remove the unexfoliated crystals, the dispersion was centrifuged at 1,968×*g*. The supernatant was subsequently centrifuged and washed twice with isopropanol to remove the residual polyvinylpyrrolidone. After rinsing, the MoS_2 sheets were redispersed in isopropanol at an optimized concentration.

For printing the SEA layer, the precursor solution was injected by a syringe pump at the rate of 2.5 ml min^{-1} into the slot-die head and out of the slot at the bottom. To slot-die coat the solution on the desired substrates (p-doped 5-inch silicon wafer and ITO/glass), the stage of the slot-die coater was transported at a constant rate of 10 mm s^{-1}, followed by sintering for 2 h at 500 °C in a furnace. To prepare Al_2O_3 samples, the precursor solution was spin coated onto ultraviolet-treated p-doped silicon wafers (4,000 r.p.m. for 30 s) followed by thermal annealing for 2 h at 500 °C in a furnace. ALD-deposited Al_2O_3 was prepared by standard ALD at a processing temperature of 100 °C.

MoS_2 sheet dispersion solutions were slot-die coated on top of dielectric layers with a syringe-pump injection rate of 2.5 ml min^{-1} and stage transport speed of 10 mm s^{-1}. After MoS_2 sheet solutions were successfully coated, procedures to enhance the electrical properties of the semiconductor film were performed, namely, a soft baking process of 60 °C for 2 min, chemical doping by 10 mg ml^{-1} of TFSI (Sigma-Aldrich) in 1,2-dichloroehtane (Sigma-Aldrich) solvent for 30 min and thermal annealing at 250 °C for 30 min. Both chemical doping by TFSI and thermal annealing were performed in an argon-filled glove box. To form channel arrays, MoS_2 films were covered by a photoresist mask (AZ 5214E) patterned by conventional photolithography and then processed with reactive ion etching followed by photoresist lift-off. Source/drain electrodes were created by the sequential thermal deposition of Cr (3 nm) and Au (30 nm) metal layers through a photolithographically patterned photoresist layer. Afterwards, a lift-off process was applied. The channel length and width were each defined as 10 μm for all the devices. To fabricate logic gates, an additional photolithography patterning of ITO local gate electrodes and SEA was conducted before and after coating the SEA.

Characterization

The surface topography and work function of the MoS_2 thin film were characterized using atomic force microscopy and KPFM, respectively (Park Systems NX10). The elemental composition and chemical structure were investigated using X-ray photoelectron spectroscopy (ESCALAB 250Xi, Thermo Fisher Scientific) and Raman/photoluminescence spectroscopy (MAPLE-II). The electrical impedances of SEA, solution-processed Al_2O_3 and ALD-deposited Al_2O_3 were measured using a VersaSTAT 4 potentiostat based on the metal–insulator–metal structure. The specific capacitance of the ITO–SEA–MoS_2 metal–insulator–semiconductor structure was measured with an inductance–capacitance–resistance meter (E4980A, Keysight). The electrical properties of the TFTs and logic gates were characterized by using a vacuum probe station (under 10^{-4} torr) and Keithley 4200 semiconductor electrometer. Hall measurements were performed using a helium cryostat with a superconducting magnet (Teslatron CF cryostat, Oxford Instruments) at 300 K. The magnetic field was applied to the device with a perpendicular direction from 0 to 4 T. Also, the magnetoresistances (R_{xx} and R_{xy}) were measured using a lock-in technique with an a.c. bias current of 100 nA. All the measurements were performed by the four-terminal method with the Hall bar devices.

Data availability

Source data are provided with this paper. The other data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Acknowledgements

This work was supported by the Basic Science Program (NRF-2020R1A2C2007819) through the National Research Foundation (NRF) of Korea funded by the Ministry of Science and ICT, Korea (J.H.C); the Creative Materials Discovery Program through the NRF funded by the Ministry of Science and ICT (NRF-2019M3D1A1078299) (J.H.C.); the Yonsei Signature Research Cluster Program of 2021 (J.H.C.); the NRF grant funded by the Korean Government (MSIT) (RS-2023-00208538) (J. Kang); and the Korea Basic Science Institute (KBSI) National Research Facilities and Equipment Center (NFEC) grant funded by the Korean Government (Ministry of Education) (2019R1A6C1010031) (J. Kang). This research was partially supported by BrainLink program funded by the Ministry of Science and ICT through the NRF of Korea (RS-2023-00237308) (J.H.C. and J. Kang).

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J.H.C. and J. Kang initiated and supervised all the research. Y.A.K. and Jihyun Kim carried out and designed most of the experimental work and data analysis. M.S.K., D.G.R., D.R. and D.W.K. assisted in the materials processing. S.B.J., Y.S., B.K., D.K. and Jeongmin Kim assisted in the electrical measurements and analysis. All authors discussed the results and contributed to the writing of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-023-00971-7.

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Peer review information *Nature Electronics* thanks the anonymous reviewers for their contribution to the peer review of this work.